UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,262	08/06/2001	Srikanth Nagaraja	1156-2	2476

23869 7590 11/26/2003

HOFFMANN & BARON, LLP
6900 JERICHO TURNPIKE
SYOSSET, NY 11791

EXAMINER	
ABEL JALIL, NEVEEN	

ART UNIT	PAPER NUMBER
2175	12

DATE MAILED: 11/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/923,262	NAGARAJA, SRIKANTH	
	Examiner	Art Unit	
	Neveen Abel-Jalil	2175	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) *31-44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-30 and 45-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The response filed on October 16, 2003 has been received and entered. Claims 1-60 are pending in the application. Of the above claims, 1-15, and 31-44 are withdrawn from consideration.

2. Applicant's election of claims 15-30, and 45-60 in Paper No. 11 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 15-30, and 45-60 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The claimed recitation of "operational plane memory" claimed in claim 15, lines 6-8, claim 16, lines 10-12, claim 45, lines 10-13, and claim 46, lines 15-17 is subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. On page 4,

lines 16-17, the specification mentions the term "operational plane memory". However, the specification does not define or describe what is "operational plane memory." It is unclear to the Examiner as what is the difference between "operational plane memory" and "memory"?

Claims 17-30, and 47-60 are dependent from independent claims 15, 16, 45, and 46 and therefore contain the same deficiency as specified above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 15-30, and 45-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Melli et al. (U.S. Pub. No. 2002/0111699 A1) in view of Dyer et al. (U.S. Patent No. 6,625,592 B1) as best taught and understood.

As to claim 15, Melli et al. discloses a method of performing a search function in an integrated circuit (See page 3, paragraph 0030), the method comprising the steps of:

storing a table into a table memory in the integrated circuit (See page 3, paragraphs 0030-0034);

inputting a search key (See page 2, paragraphs 0024-0026);

performing at least one search function on the table in the operational plane memory using the search key (See page 3, paragraph 0032, also see page 2, paragraph 0024).

Melli et al. does not teach transferring substantially simultaneously the table in parallel from the table memory to an operational plane memory in the integrated circuit; and

outputting a result of the at least one search function.

Dyer et al. teaches transferring substantially simultaneously the table in parallel from the table memory to an operational plane memory in the integrated circuit (See column 5, lines 4-45); and outputting a result of the at least one search function (See column 5, lines 35-46).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Melli et al. to include transferring substantially simultaneously the table in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function.

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Melli et al. by the teaching of Dyer et al. to include transferring substantially simultaneously the table in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function because it allows for faster processing and more efficient use of the integrated circuitry in a computer.

As to claim 16, Melli et al. discloses a method of performing a search function in an integrated circuit (See page 3, paragraph 0030), the method comprising the steps of:

storing a plurality of tables into a table memory in the integrated circuit (See page 3, paragraphs 0030-0034);

inputting a table identifier, the table identifier being representative of one of the plurality of sorted tables (See page 3, paragraph 0030, and also see pages 3-4, paragraph 0035);

inputting a search key (See page 2, paragraphs 0024-0026);

performing at least one search function on the at least one table in the operational plane memory using the search key (See page 3, paragraph 0032, also see page 2, paragraph 0024).

Melli et al. does not teach transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and

outputting a result of the at least one search function.

Dyer et al. teaches transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit (See column 5, lines 4-45); and

outputting a result of the at least one search function (See column 5, lines 35-46).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Melli et al. to include transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function.

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Melli et al. by the teaching of Dyer et al. to include transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the

integrated circuit; and outputting a result of the at least one search function because it allows for faster processing and more efficient use of the integrated circuitry in a computer.

As to claim 17, Melli et al. as modified discloses comprising the step of coupling the integrated circuit to at least one of a microprocessor (See Dyer et al. column 3, lines 57-678, and see Dyer et al. column 4, lines 1-5), a microcontroller, and an application specific integrated circuit (ASIC) (See Melli et al. page 3, paragraph 0030).

As to claim 18, Melli et al. as modified discloses comprising the step of arranging at least one of the table memory and the operational plane memory as a multi-dimensional array of memory (See Dyer et al. column 5, lines 47-64, also see Melli et al. page 3, paragraphs 0028-0030).

As to claim 19, Melli et al. as modified discloses comprising the step of arranging at least one of the table memory and the operational plane memory in at least one column, at least one row, and at least one table (See pages 3-4, paragraphs 0035-0036).

As to claim 20, Melli et al. as modified discloses comprising the steps of:

arranging the at least one column as an array of bytes (See Dyer et al. column 4, lines 22-61);

arranging the at least one row as an array of columns (See Dyer et al. column 3, lines 8-56); and

arranging the at least one table as an array of rows (See Dyer et al. figure 3).

As to claim 21, Melli et al. as modified discloses comprising the step of storing the result in at least one register in the integrated circuit, the at least one register being accessible to at least one device external to the integrated circuit (See Dyer et al. column 3, lines 32-44, also see Dyer et al. column 5, lines 1-34).

As to claim 22, Melli et al. as modified discloses comprising the steps of:

inputting a command to at least one register in the integrated circuit (See Dyer et al. column 3, lines 57-67, and see Dyer et al. column 4, lines 1-41);

interpreting the command by the integrated circuit (See page 2, paragraphs 0014-0019); and

initiating an action in the integrated circuit in response to the command (See page 4, paragraphs 0035-0036, wherein "response to command" reads on "process the request").

As to claim 23, Melli et al. as modified discloses wherein the command is representative of one of specifying a portion of the storage circuit in which to store at least one of the plurality of tables (See page 1, paragraph 0002), initiating storage of the plurality of tables in the storage circuit, specifying the at least one table stored in the storage circuit on which to perform the at least one search function (See page 3, paragraphs 0029-0030), specifying at least one search key, specifying the at least one search function, and initiating the at least one search function (See

page 3, paragraphs 0032-0034).

As to claim 24, Melli et al. as modified discloses comprising the step of inputting a search function identifier, the search function identifier being representative of one of the plurality of search functions, the integrated circuit, performing the at least one search function represented by the search function identifier (See page 3, paragraphs 0029-0032, also see Dyer et al. column 3, lines 32-67).

As to claim 25, Melli et al. as modified discloses wherein the at least one table includes a plurality of entries, the step of performing the at least one search function being performed in parallel on the plurality of entries of the at least one table (See Dyer et al. column 5, lines 1-34).

As to claim 26, Melli et al. as modified discloses wherein the at least one table includes a plurality of entries, the result including at least one of the plurality of entries that equals a search key (See Dyer et al. column 5, lines 65-67, and see Dyer et al. column 6, lines 1-16).

As to claim 27, Melli et al. as modified discloses wherein the at least one table includes a plurality of entries, the result including at least two of the plurality of entries between which a search key is located (See page 2, paragraphs 0020-0021).

As to claim 28, Melli et al. as modified discloses wherein the at least one search function performed includes at least one of a sequential and a parallel N-ary search (See page 3,

paragraphs 0030-0031).

As to claim 29, Melli et al. as modified discloses wherein the step of transferring one of the plurality of tables substantially simultaneously in parallel (See Dyer et al. column 5, lines 1-34) from the table memory to the operational plane memory in the integrated circuit is performed in response to the integrated circuit receiving an initiate search command (See page 2, paragraphs 0014-0020, also see page 2, paragraphs 0026, and see page 3, paragraph 0030).

As to claim 30, Melli et al. as modified discloses comprising the step of modifying the at least one table while the at least one table is in the operational plane memory (See page 2, paragraph 0022, also see Dyer et al. column 7, lines 34-65).

As to claim 45, Melli et al. discloses a method of performing a search function, the method comprising the steps of:

inputting unsorted entries (See page 2, paragraphs 0020-0021, wherein "unsorted" reads on "generic");

performing a hash function on the unsorted entries, the hash function arranging the unsorted entries into a sorted table (See pages 3-4, paragraph 0035);

storing the sorted table into a table memory in an integrated circuit (See page 3, paragraphs 0030-0034);

inputting a search key (See page 2, paragraphs 0024-0026);

performing at least one search function on the sorted table in the operational plane memory using the search key (See page 3, paragraph 0032, also see page 2, paragraph 0024).

Melli et al. does not teach transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and

outputting a result of the at least one search function.

Dyer et al. teaches transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit (See column 5, lines 4-45); and

outputting a result of the at least one search function (See column 5, lines 35-46).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Melli et al. to include transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function.

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Melli et al. by the teaching of Dyer et al. to include transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function because it allows for faster processing and more efficient use of the integrated circuitry in a computer.

As to claim 46, Melli et al. discloses a method of performing a search function, the method comprising the steps of:

inputting unsorted entries (See page 2, paragraphs 0020-0021, wherein "unsorted" reads on "generic");

performing a first hash function on the unsorted entries, the first hash function arranging the unsorted entries into a plurality of sorted tables (See pages 3-4, paragraph 0035);

storing the plurality of sorted tables into a table memory in an integrated circuit (See page 3, paragraphs 0030-0034);

inputting a search key (See page 2, paragraphs 0024-0026);

performing a second hash function on the search key, the second hash function outputting a table identifier (See page 3, paragraph 0032, also see page 2, paragraph 0024),

the table identifier being representative of one of the plurality of sorted tables in which the search key is likely to be found (See page 3, paragraphs 0029-0030, also see figure 5, 262);

performing at least one search function on the at least one table in the operational plane memory using the search key (See page 2, paragraphs 0024-0025).

Melli et al. does not teach transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and

outputting a result of the at least one search function.

Dyer et al. teaches transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit (See column 5, lines 4-45); and

outputting a result of the at least one search function (See column 5, lines 35-46).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Melli et al. to include transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function.

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Melli et al. by the teaching of Dyer et al. to include transferring substantially simultaneously at least one of the plurality of tables represented by the table identifier in parallel from the table memory to an operational plane memory in the integrated circuit; and outputting a result of the at least one search function because it allows for faster processing and more efficient use of the integrated circuitry in a computer.

As to claim 47, Melli et al. as modified discloses wherein the steps of performing a first hash function and performing a second hash function are performed by at least one of a microprocessor (See Dyer et al. column 4, lines 1-5), a microcontroller, and an application specific integrated circuit (ASIC) (See Melli et al. page 3, paragraph 0030).

As to claim 48, Melli et al. as modified discloses comprising the step of arranging at least one of the table memory and the operational plane memory as a multi-dimensional array of memory (See Dyer et al. column 7, lines 21-33, also see Dyer et al. column 8, claim 1 language).

As to claim 49, Melli et al. as modified discloses comprising the step of arranging at least one of the table memory and the operational plane memory in at least one column, at least one row, and at least one table (See pages 3-4, paragraphs 0035-0036).

As to claim 50, Melli et al. as modified discloses comprising the steps of:

arranging the at least one column as an array of bytes (See Dyer et al. column 4, lines 22-61);

arranging the at least one row as an array of columns (See Dyer et al. column 3, lines 8-56); and

arranging the at least one table as an array of rows (See Dyer et al. figure 3).

As to claim 51, Melli et al. as modified discloses comprising the step of storing the result in at least one register in the integrated circuit, the at least one register being accessible to at least one device external to the integrated circuit (See Dyer et al. column 5, lines 1-34).

As to claim 52, Melli et al. as modified discloses comprising the steps of:

inputting a command to at least one register in the integrated circuit (See Dyer et al. column 3, lines 57-67, and see Dyer et al. column 4, lines 1-41);

interpreting the command by the integrated circuit (See page 2, paragraphs 0014-0019); and

initiating an action in the integrated circuit in response to the command (See page 4, paragraphs 0035-0036, wherein "response to command" reads on "process the request").

As to claim 53, Melli et al. as modified discloses wherein the command is representative of one of specifying a portion of the storage circuit in which to store at least one of the plurality of tables (See page 1, paragraph 0002), initiating storage of the plurality of tables in the storage circuit, specifying the at least one table stored in the storage circuit on which to perform the at least one search function (See page 3, paragraphs 0029-0030), specifying at least one search key, specifying the at least one search function, and initiating the at least one search function (See page 3, paragraphs 0032-0034).

As to claim 54, Melli et al. as modified discloses the method further comprising the step of inputting a search function identifier, the search function identifier being representative of one of the plurality of search functions, the integrated circuit performing the at least one search function represented by the search function identifier (See page 3, paragraphs 0029-0032, also see Dyer et al. column 3, lines 32-67).

As to claim 55, Melli et al. as modified discloses wherein the at least one table includes a plurality of entries, the step of performing the at least one search function being performed in parallel on the plurality of entries of the at least one table (See Dyer et al. column 5, lines 1-34).

As to claim 56, Melli et al. as modified discloses wherein the at least one table includes a plurality of entries, the result including at least one of the plurality of entries that equals a search key (See Dyer et al. column 5, lines 65-67, and see Dyer et al. column 6, lines 1-16).

As to claim 57, Melli et al. as modified discloses wherein the at least one table includes a plurality of entries, the result including at least two of the plurality of entries between which a search key is located (See page 2, paragraphs 0020-0021).

As to claim 58, Melli et al. as modified discloses wherein the at least one search function performed includes at least one of a sequential and a parallel N-ary search (See Dyer et al. column 7, lines 21-33, also see Dyer et al. column 8, claim 1 language).

As to claim 59, Melli et al. as modified discloses wherein the step of transferring one of the plurality of tables substantially simultaneously in parallel (See Dyer et al. column 5, lines 1-34) from the table memory to the operational plane memory in the integrated circuit is performed in response to the integrated circuit receiving an initiate search command (See page 2, paragraphs 0014-0020, also see page 2, paragraphs 0026, and see page 3, paragraph 0030).

As to claim 60, Melli et al. as modified discloses comprising the step of modifying the at least one table while the at least one table is in the operational plane memory (See page 2, paragraph 0022, also see Dyer et al. column 7, lines 34-65).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Choe (U.S. Pub. No. 2002/0118682 A1) teaches method for performing high-speed IP route lookup.

Guha (U.S. Patent No. 6,539,373 B1) teaches contextual searching by determining intersections of search results.

Narad et al. (U.S. Patent No. 6,157,955) teaches packet processing system including a policy engine having a classification unit.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Neveen Abel-Jalil whose telephone number is 703-305-8114. The examiner can normally be reached on 8:00AM-4: 30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on 703-305-3830. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Charles Rones

CHARLES RONES
PRIMARY EXAMINER

Neveen Abel-Jalil
November 12, 2003